R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The Applicant thanks Examiner Suryawanshi for the indications of allowable matter in claim 10.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, in FIGS. 1 and 6, as originally filed. New claim 21 incorporates the allowable matter of the original claim 10 and intervening claim 9. New claim 22 is the gating circuit from the original claim 9. New claim 23 is the original claim 10 in method form. Thus, no new matter has been added.

SUPPORT FOR THE DRAWING AMENDMENT

Support for the drawing amendment may be found in the specification, for example, on page 9, lines 5-8, as originally filed. Reference 104 has been added. Thus, no new matter has been added.

OBJECTION TO THE DRAWINGS

The objection to the drawings has been obviated by the proposed amendment and should be withdrawn.

A reference number 104 has been added to the multiplexer circuit in FIG. 1, as shown in red and submitted herein. Approval of the proposed drawing amendment is respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 7, 8, 11, 17, 18 and 20 under 35 U.S.C. §102(e) as being anticipated by Melava et al. '674 (hereafter Melava) has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Melava concerns a fractional multimodulus prescaler (Title).

Claim 1 provides (A) a first circuit configured to generate a plurality of control signals in response to a first clock signal having a first frequency and (B) a multiplexer configured to multiplex a plurality of data signals in response to the control signals to present a second clock signal having a second frequency that is a non-integer fraction of the first frequency. The Office Action asserts on page 3 that FIG. 4 of Melava shows a component signal composer block 402 similar to the claimed first circuit and a phase selector block 403 similar to the claimed multiplexer. Therefore, the Office appears to be arguing that (i) K component signals presented by the block 402 of Melava are similar to the claimed plurality of control signals and (ii)

the control signals of Melava are similar to the claimed data signals. However, FIG. 5 of Melava appears to show that the block 403 (asserted similar to the claimed multiplexer circuit) actually multiplexes the K component signals (asserted similar to the claimed control signals) in response to the control signals of Melava (asserted similar to the claimed data signals). The block 403 of Melava appears to be multiplexing different signals than as claimed. Therefore, Melava does not appear to disclose or suggest (A) a first circuit configured to generate a plurality of control signals in response to a first clock signal having a first frequency and (B) a multiplexer configured to multiplex a plurality of data signals in response to the control signals to present a second clock signal having a second frequency that is a non-integer fraction of the first frequency as presently claimed.

Claim 1 further provides a second circuit configured to generate the data signals in response to the second clock signal. Assuming, *arguendo*, that the block 403 of Melava somehow multiplexes the claimed data signals (for which Applicant's representative does not necessarily agree), Melava appears to be silent regarding the K component signals of Melava being generated by a post-divider block 404 of Melava (asserted similar to the claimed second circuit). Therefore, Melava does not appear to disclose or suggest a second circuit configured to generate the data signals in response to the second clock signal as presently

claimed. Claims 11 and 20 provide language similar to claim 1. As such, the claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 further provides a second circuit configured to present the data signals directly to the multiplexer. In contrast, the block 404 of Melava (asserted similar to the claimed second circuit) does not appear to present any signals directly to the block 403 of Melava (asserted similar to the claimed multiplexer). Therefore, Melava does not appear to disclose or suggest a second circuit configured to present the data signals directly to the multiplexer as presently claimed. Claim 11 provides language similar to claim 1. As such, claims 1 and 11 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 7 provides that the first circuit is configured to present one of the control signals in an active state at a time. Applicant's representative respectfully traverses the assertion on page 5 of the Office Action that operation of the block 403 of Melava inherently requires at least one of the K component signals be in an active state at a time. MPEP §2112 states:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. " *Ex parte Levy* 17 USPQ2d 1461, 1464, 1464 (Bd. Pat. App. & Inter. 1990)(emphasis in original)

However, no evidence or convincing line of reasoning has been provided in the Office Action why the operation of the block 403 necessarily results in the block 402 generating at least one of the K component signal in an active state at a time. Since inherency has not been established, *prima facie* anticipation has not been established. Claim 17 provides language similar to claim 7. As such, claims 7 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

Claims 8 and 18 depend directly from claims 1 and 11, which are now believed to be allowable. As such, the rejection of claims 8 and 18 should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2-6, 9, 12-16 and 19 under 35 U.S.C. §103(a) as being unpatentable over Melava is respectfully traversed and should be withdrawn.

Melava concerns a fractional multimodulus prescaler (Title). In contrast, the Office Action fails to provide clear and particular motivation to modify Melava. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (MPEP §2143.01). Therefore, *prima facie* obviousness has not been established for lack of evidence for motivation. The Examiner is respectfully requested to either (i) provide clear and particular evidence why one of ordinary skill in

the art would be motivated to make the modifications to Melava as suggested in the Office Action or (ii) withdraw the rejection.

Claim 2 provides that the second circuit is configured to sequence the plurality of data signals through a plurality of patterns response to the second clock signal. In contrast, the Office Action fails to establish that the block 404 of Melava generates any signals similar to the claimed plurality of data signals. In particular, none of the signals generated by the block 404 of Melava appear to be multiplexed by the block 403 of Melava (asserted similar to the claimed multiplexer). The assertions on page 6 of the Office Action that it would have been obvious to modify the block 404 of Melava "as needed" is moot for lack of signals back to the block 403. Therefore, *prima facie* obviousness has not been established for lack of evidence that the proposed modified Melava teaches all of the claim limitations. Claim 12 provides language similar to claim 2. As such, the rejection of claims 2 and 12 should be withdrawn.

Claim 4 provides that the second circuit is configured to present the data signals in a second predetermined pattern such that the second frequency equals the first frequency. In contrast, Melava appears to be silent regarding a frequency division of one. Therefore, Melava does not appear to teach or suggest a second circuit configured to present a plurality of data signals in a

second predetermined pattern such that a second frequency equals a first frequency as presently claimed.

Furthermore, the Office Action makes no arguments that Melava could be obviously modified to divide by one. Therefore, *prima facie* obviousness has not been established for lack of evidence that the proposed modified Melava teaches all of the claim limitations. Claim 14 provides language similar to claim 4. As such, the rejection of claims 4 and 14 should be withdrawn.

Claim 5 provides a plurality of latches configured to latch the data signal presented by the second circuit. In contrast, the Office Action admits that Melava does not mention latches. Therefore, Melava does not teach or suggest a plurality of latches configured to latch a plurality of data signal presented by a second circuit as presently claimed. Claim 15 provides language similar to claim 5. As such, the rejection of claims 5 and 15 should be withdrawn.

Claim 6 provides that the latches are configured to sample the data signals in a staggered order in response to the control signals. In contrast, the Office Action admits that Melava does not mention latches. Therefore, Melava does not teach or suggest a plurality of latches configured to sample a plurality of data signals in a staggered order in response to a plurality of control signals as presently claimed.

Furthermore, the Office Action makes no arguments regarding the proposed latches sampling any signal from the block 404 (asserted similar to the claimed second circuit) in response to the K component signals (asserted similar to the claimed control signals). Therefore, *prima facie* obviousness has not been established for lack of evidence that the proposed modified Melava teaches all of the claim limitations. Claim 16 provides language similar to claim 6. As such, the rejection of claims 6 and 16 should be withdrawn.

Claim 9 provides (A) a first dividing circuit configured to divide the second clock signal by a first predetermined integer to present a third clock signal and (B) a second dividing circuit configured to divide the third clock signal by a second predetermined integer to present a fourth clock signal. In contrast, the Office Action admits that Melava does not mention a first dividing circuit and a second dividing circuit. Therefore Melava does not teach or suggest (A) a first dividing circuit configured to divide the second clock signal by a first predetermined integer to present a third clock signal and (B) a second dividing circuit configured to divide the third clock signal by a second predetermined integer to present a fourth clock signal as presently claimed.

Furthermore, the Office Action makes no arguments regarding the claimed first predetermined integer and the second

predetermined integer. Therefore, *prima facie* obviousness has not been established for lack of evidence that the proposed modified Melava teaches all of the claim limitations. Claim 19 provides language similar to claim 9. As such, the rejection of claims 9 and 19 should be withdrawn.

Claims 3 and 13 depend either directly or indirectly from claims 1 and 11, which are now believed to be allowable. Therefore, claims 3 and 13 are fully patentable over the cited reference and the rejection should be withdrawn.

The allowable matter of claim 10 has been rewritten into independent form in new claim 21. As such, claim 10 should be allowed.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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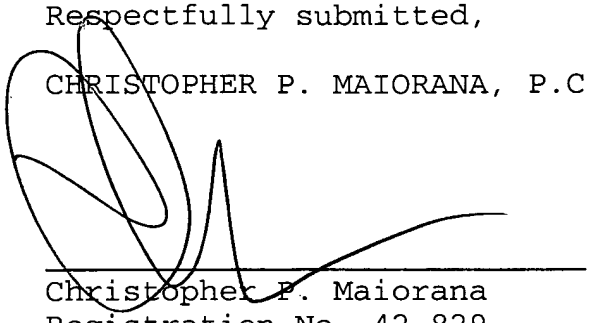

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